

## Introduction

The I<sup>2</sup>C ID Module has been developed primarily for harness & adaptor identification. Due to its small size, the module can be fitted to any test harness or adaptor and allows users to store specific data relating to the hardware. 256Kbytes of EEPROM data can be stored.

If the I<sup>2</sup>C ID Module is used along with the Peak I<sup>2</sup>C Mux Module, communications will still be stable up to 30 metres away from the I<sup>2</sup>C master making it ideal for large factory installations.

## Key Features

- Robust, Flexible Design
- Low Cost
- Small Size
- Compatible with any I<sup>2</sup>C interface
- Hardware Write Protect
- Up to Eight Devices on One I<sup>2</sup>C Bus
- 256kbytes Data Storage
- All Components Fully Traceable

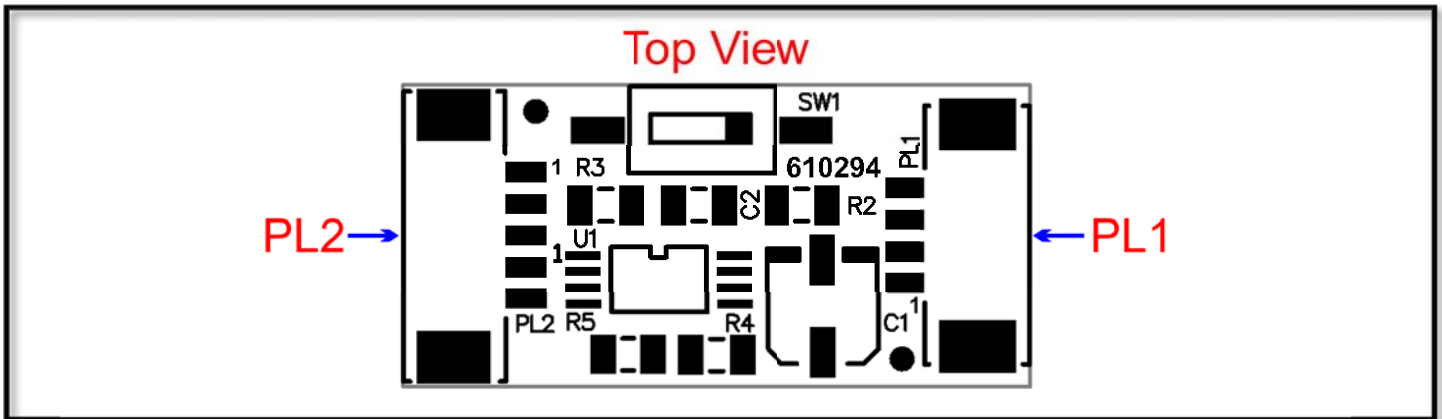


## Specifications

Parameter	Min	Typ	Max	Unit
Supply Voltage	2.5	-	5.5	VDC
Supply Current[1]	0.001	0.005	3	mA
Operating Temperature	-40	-	+100	°C
I <sup>2</sup> C Bus Speed	37	100	400	kbit/s
I <sup>2</sup> C HIGH-level Input Voltage	0.7	-	5.5	VDC
I <sup>2</sup> C LOW-level Input Voltage	-0.5	-	0.3	VDC
Memory	-	-	256	Kbytes
Data Erase/Write Cycles	-	-	>1	Million
Data Retention	-	-	>200	Years

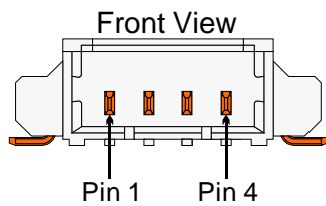
[1] Based on 5.5VDC supply

Connectivity



PL1

- Pin 1 = +V
- Pin 2 = SCL (I<sup>2</sup>C Clock)
- Pin 3 = 0V
- Pin 4 = SDA (I<sup>2</sup>C Data)



Mating Connector:

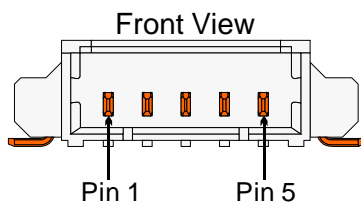
Molex PicoBlade – Part No: 51021-0400

Crimp Contacts:

Molex PicoBlade – Part No: 50058-8100

PL2

- Pin 1 = +V
- Pin 2 = A0
- Pin 3 = A1
- Pin 4 = A2
- Pin 5 = 0V



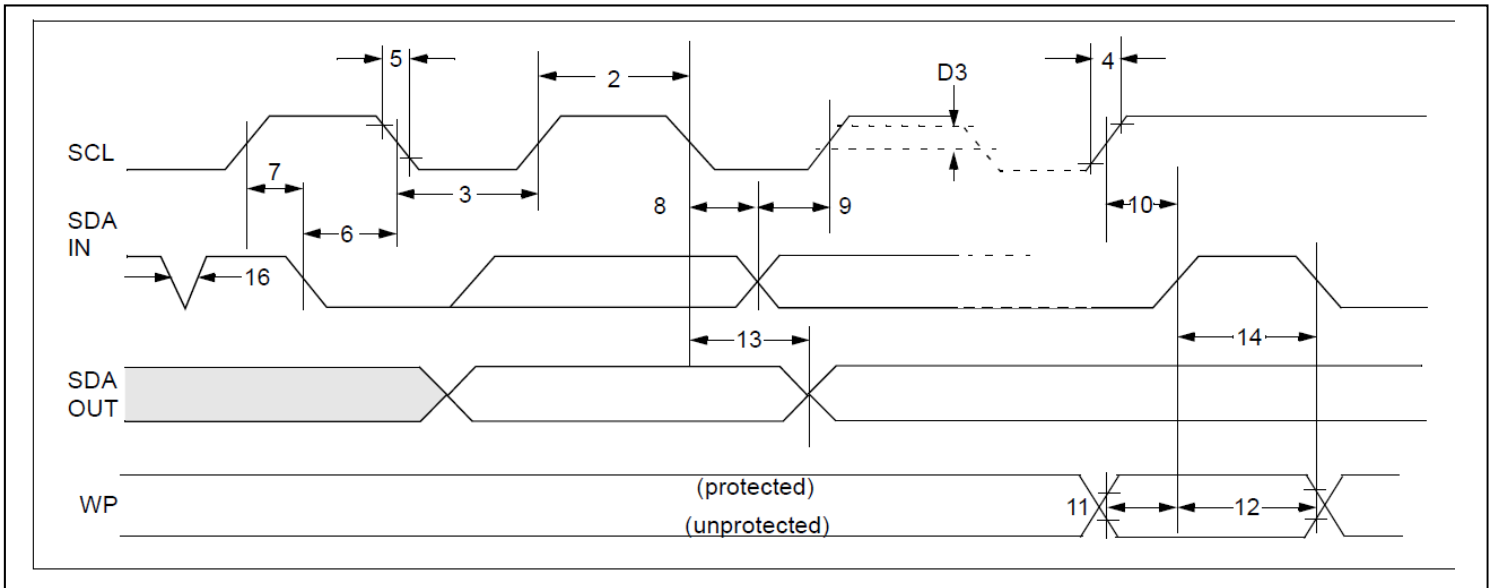
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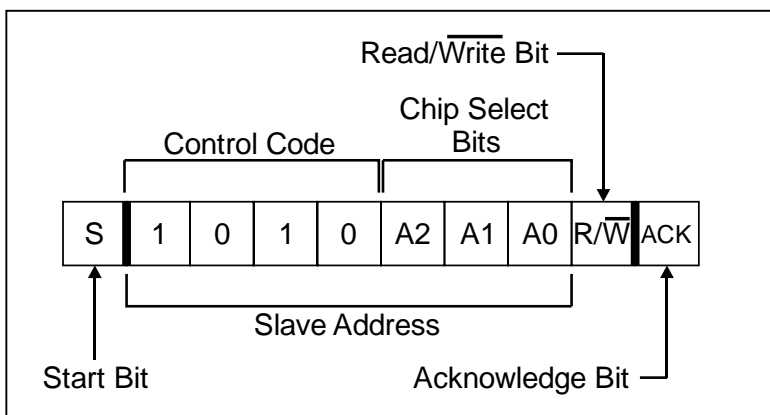
### I<sup>2</sup>C Bus Timing



### Addressing

The default address for the I<sup>2</sup>C ID Module is set in hardware to 1010000. This can be modified by looping back +V to the three chip select connections (A0-A2) on PL2. The chip select lines are internally pulled low.

If more than one device is used on the same I<sup>2</sup>C bus simultaneously the chip select lines must be used to change the slave address so that each I<sup>2</sup>C ID Module has a unique address. A maximum of eight devices can be used on one I<sup>2</sup>C bus.



### Write Protection

The I<sup>2</sup>C ID Module is fitted with a write protection switch labelled WP. If the switch is enabled all writes to the module are disabled, reads will still function as normal

## Memory Map

The I<sup>2</sup>C ID Module memory has 500 pages with 64 bytes of data on each, as shown below.

<b>Memory Map</b>									
<b>Page</b>	<b>1</b>	<b>2</b>	<b>3</b>	<b>4</b>	<b>5</b>	<b>6</b>	<b>-</b>	<b>64</b>	<b>Byte</b>
<b>0</b>	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	
<b>1</b>	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	
<b>2</b>	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	
<b>3</b>	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	
<b>4</b>	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	
<b>5</b>	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	
<b>6</b>	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	
<b>7</b>	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	
<b>8</b>	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	
<b>9</b>	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	
<b>10</b>	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	
<b>11</b>	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	
<b>12</b>	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	
<b>-</b>	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	
<b>500</b>	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	

## Write Operation

Note: All commands are based on the I<sup>2</sup>C ID Module default address.

### 1.0.0 – Byte Write

To write bytes of data to the I<sup>2</sup>C ID Module the following commands need to be sent:

The 1 <sup>st</sup> byte (10100000, 0xA0)	Address the I <sup>2</sup> C ID Module plus 0 (first 7 bits = slave address, last bit (0) = write)
The 2 <sup>nd</sup> byte (????????, ?)	Memory address high byte
The 3 <sup>rd</sup> byte (????????, ?)	Memory address low byte
Data Bytes	Data
Stop	

Example:

0xA0, 0x00, 0x00, Data = Addressing byte 1 of page 1

If more than 64 bytes of data are sent the device will automatically roll over to the next page e.g. If 100 bytes of data are sent to page 1, page 1 will contain the first 64 bytes and page 2 will contain the last 36 bytes.

### 1.0.1 – Page Write

To write a complete page of data to the I<sup>2</sup>C ID Module the following commands need to be sent:

Note: A complete page consists of 64 bytes, if less than 64 bytes are sent, the remaining bytes will be refreshed.

The 1 <sup>st</sup> byte (10100000, 0xA0)	Address the I <sup>2</sup> C ID Module plus 0 (first 7 bits = slave address, last bit (0) = write)
The 2 <sup>nd</sup> byte (????????, ?)	Memory address high byte
The 3 <sup>rd</sup> byte (????????, ?)	Memory address low byte
Data Bytes (64 maximum)	Data
Stop	

Example:

0xA0, 0x00, 0x00, Data = Addressing Page 0

0xA0, 0x00, 0x01, Data = Addressing Page 1

0xA0, 0x01, 0xF4, Data = Addressing Page 500

## Read Operation

Note: All commands are based on the I<sup>2</sup>C ID Module default address.

### 1.2.0 – Current Address Read

This function can be used to read the next byte from a previous read. E.g. if page 1 byte 3 was the last byte read from the device the following command will read page 1 byte 4. After this the address is internally incremented by 1 so if the command is sent again it will read from the next byte in sequence.

The 1 <sup>st</sup> byte (10100001, 0xA1)	Address the I <sup>2</sup> C ID Module plus 0 (first 7 bits = slave address, last bit (1) = read)
Read Data Byte	Read the data back.
Stop	

### 1.3.0 – Random Read

If you need to read data from a random location the following commands must be sent.

First the location address will need to be set:

The 1 <sup>st</sup> byte (10100000, 0xA0)	Address the I <sup>2</sup> C ID Module plus 0 (first 7 bits = slave address, last bit (0) = write)
The 2 <sup>nd</sup> byte (????????, ?)	Memory address high byte
The 3 <sup>rd</sup> byte (????????, ?)	Memory address low byte
Stop	

Then the data can be read by the following command:

The 4 <sup>th</sup> byte (10100001, 0xA1)	Address the I <sup>2</sup> C ID Module plus 0 (first 7 bits = slave address, last bit (1) = read)
Read Data Byte	Read the data back.
Stop	

After a random read command, the internal address counter will point to the address location following the one that was just read.

### 1.4.0 – Sequential Read

A sequential read allows users to define a start address as a random read does but allows multiple bytes to be read back with a single command by sending acknowledgements between the bytes received.

First the location address will need to be set:

The 1 <sup>st</sup> byte (10100000, 0xA0)	Address the I <sup>2</sup> C ID Module plus 0 (first 7 bits = slave address, last bit (0) = write)
The 2 <sup>nd</sup> byte (????????, ?)	Memory address high byte
The 3 <sup>rd</sup> byte (????????, ?)	Memory address low byte
Stop	

Then the data can be read by the following command:

The 4 <sup>th</sup> byte (10100001, 0xA1)	Address the I <sup>2</sup> C ID Module plus 0 (first 7 bits = slave address, last bit (1) = read)
Read Data Byte	Read the data back.
Acknowledge	
Read Data Byte	Read the data back.
Etc.	
Stop	

After each acknowledge, the internal address counter will point to the address location following the one that was just read.